

# Dense and Highly Elastic Compressible MicroInterconnects (CMIs) for Electronic Microsystems

Paul K. Jo, Muneeb Zia, Joe L. Gonzalez, and Muhammed S. Bakir

School of Electrical and Computer Engineering

Georgia Institute of Technology

Atlanta, GA 30318, USA

Paul.Jo@gatech.edu

**Abstract**— In this paper, dense, highly elastic compressible microinterconnects (CMIs) are presented as an enabling technology for next generation sockets, probe cards and heterogeneous integrated systems. Free-standing CMIs with 75  $\mu\text{m}$  height are fabricated using a thick sacrificial photoresist layer with an upward curved sidewall profile. The CMIs show a 45  $\mu\text{m}$  vertical elastic range of motion. The fabricated CMIs have an in-line pitch of 150  $\mu\text{m}$ , mechanical compliance of 9.2  $\text{mm/N}$ , and exhibit elastic motion for up to 5,000 indentation cycles. The smallest in-line pitch of CMIs demonstrated is 40  $\mu\text{m}$ . The average post-assembly resistance of the CMIs, including the contact resistance, was measured to be 176.3  $\text{m}\Omega$ .

**Keywords**—Compliant Interconnects, 2.5D/3D Package Assembly, Wafer Probe Cards, Sockets

## I. INTRODUCTION

Compliant interconnects have been widely used in various electronic applications including wafer probe testing [1], [2], Land Grid Array (LGA) socket technology [3]-[5], cell-culturing bio-applications [6], microchip packaging [7]-[9], and MEMS applications [10]. However, continued scaling and recent advances in 2.5D and 3D integration have surfaced new set of challenges that remain unmet with the current state of the art. For example, the high-end server market requires sockets that can cater to the increasing density of connections while maintaining the overall loading force [11]. Furthermore, as the data rates increase, there is a need to reduce the overall electrical length of the connectors to minimize loss [11]. Likewise, although 3D integration utilizing through-silicon-vias has allowed stacking of dice to achieve densities that were unprecedented before, it has also brought a critical challenge in the testing domain; known good dice (KGD) are needed to increase the 3D IC yield and thus, there is a need to do pre-bond testing [12]. However, the microbumps on the dice are extremely dense with a pitch of 20 to 40  $\mu\text{m}$  and thus possibly difficult to probe [12]. Although workarounds to the approach have been proposed by including dedicated pads for testing, this requires additional design and processing steps as well as infringes upon valuable silicon real estate [12]. Thus, the ability to probe directly onto the scaled bumps poses similar challenges to that of the socket where scalable pitch, low-contact resistance and high compliance interconnects are required as the probe tips in order to make good electrical connection to the bumps without causing mechanical damage. Furthermore, such an interconnect can enable

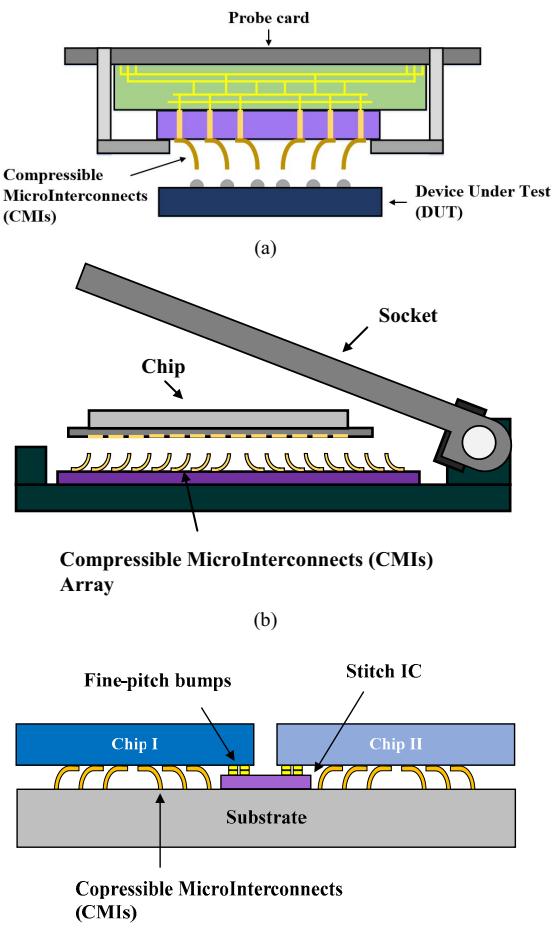


Fig. 1. Various electronic microsystem applications with compressible microinterconnects (CMIs); (a) wafer probe card, (b) socketed package, and (c) heterogeneous multi-die integration platform using a stitch IC

seamless integration of multiple dice in a heterogeneous integrated system where different substrates might have to be used; CTE mismatch or height variations can be compensated by using such an interconnect while maintaining good electrical connection.

In this paper, we present dense, highly elastic compressible microinterconnects (CMIs) as an enabling

TABLE I  
COMPARISON OF COMPLIANT INTERCONNECTS

Technology	Pitch ( $\mu\text{m}$ )	Height ( $\mu\text{m}$ )	Compliance (out-of-plane) ( $\text{mm} / \text{N}$ )	Vertical range of motion ( $\mu\text{m}$ )	Attributes
<b>This work</b>	> 40	75	9.2	45	- Simple fabrication process - Large range of compliance is achievable - High elastic range of motion
<b>Rematable spring interconnects [8]</b>	180	50	218	32	- Stress engineering fabrication - High elastic range of motion
<b>Sea-of-leads (SoL) [5] [11]</b>	> 120	60 ~ 90	0.5 ~ 2	< 30	- Polymer embedded air gap
<b>G-Helix [14]</b>	100	78	14.7	-	- Simple fabrication process
<b><math>\beta</math>-Helix [15]</b>	200	110	> 7.1	-	- Large range of compliance is achievable - Simple fabrication process
<b>Mechanically flexible interconnects (MFIs) [16]</b>	> 50	65	< 5.32	< 50	- Large range of compliance is achievable - High elastic range of motion
<b>J-springs [17]</b>	40	100	> 3000	-	- Stress engineering fabrication - High elastic range of motion
<b>Intel Core i7 processor LGA socket [18] [19]</b>	1,016	-	-	-	- Injection molding manufacturing - High height & elastic range of motion - Board level application
<b>Samtec Z-ray micro interposer [19]</b>	800	1,000	0.8	203	- Injection molding manufacturing - High height & elastic range of motion - Board level application

technology to better meet the requirements of the applications discussed above. Some of the key attributes of the fabricated CMIs include: 1) lithographically-defined and CMOS compatible fabrication process, 2) high flexibility and large elastic range of motion to compensate for surface non-uniformity of the substrate, dice, or CTE mismatch induced warpage, 3) pressure-based temporary contact mechanism, which enables chips or packages to be replaced, 4) high degree of freedom in the engineering of the CMI; this includes scaling of pitch, height, compliance, and contact resistance, and 5) no reflow process is required to define the CMI shape.

Fig. 1 shows the utilization of the CMIs in the applications discussed earlier. Table I compares key attributes of various compliant interconnects in the literature and the work presented in this paper.

## II. FABRICATION

Fig. 2 illustrates the fabrication process flow of CMIs. The first step begins with surface passivation by depositing a thin silicon nitride or oxide layer on the surface of the wafer. Next, a thick sacrificial photoresist layer is spin coated onto the surface; the film thickness of the resist determines the height of the CMIs. During the lithography step, an upward-curved sidewall is patterned in order to form the CMI's body. A Ti/Cu/Ti seed layer is then deposited using sputtering followed by spray coating of another photoresist layer to form the electroplating molds. After patterning the electroplating molds, NiW is electroplated into the mold to

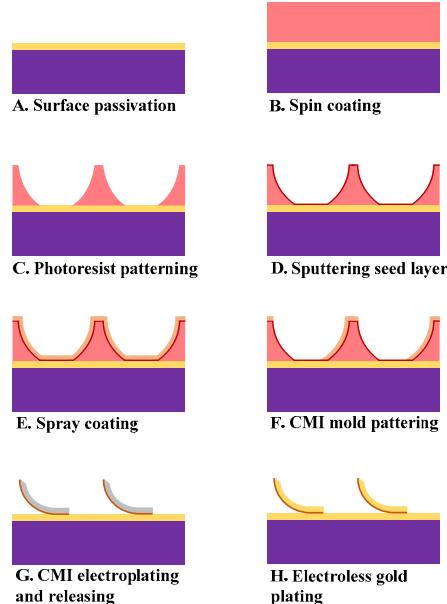


Fig. 2. Fabrication process flow

create the CMIs. NiW is used to form the CMIs since it provides better mechanical performance than Cu; the yield strength of NiW is significantly higher (up to 1.93 GPa)

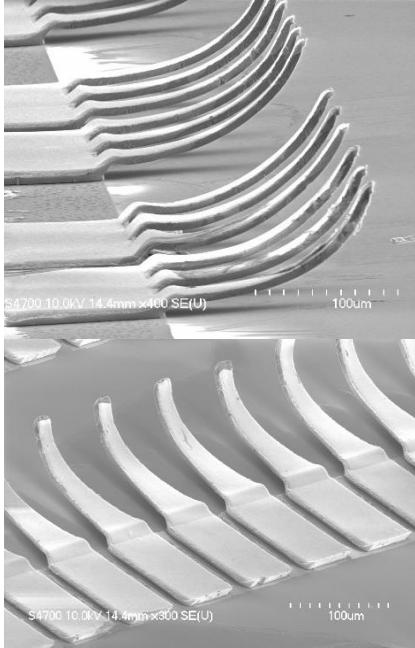


Fig. 3. SEM images of CMIs

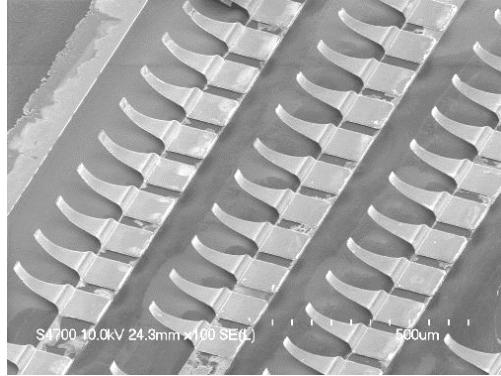


Fig. 4. SEM image of an array of CMIs

compared to Cu (136 MPa), which enables CMIs to be more durable under stress and allows for a higher vertical elastic range of motion [21], [21]. After electroplating, the spray coated photoresist layer, the Ti/Cu/Ti seed layer, and the sacrificial photoresist layer are removed leaving free-standing CMIs. Lastly, a thin gold layer is deposited on the CMI surfaces by electroless gold plating; the gold layer prevents the oxidation of the NiW and hence it enhances the electrical performance of the CMI. Fig. 3 and Fig. 4 show SEM images of the fabricated CMIs. The height of the CMIs is 75  $\mu$ m and the in-line pitch is 150  $\mu$ m. The thickness of the CMIs is approximately 10.5  $\mu$ m. However, since CMIs are lithographically-defined, the pitch of the CMIs can be scaled, and the maximum height of the CMIs can be adjusted accordingly by changing the thickness of the sacrificial

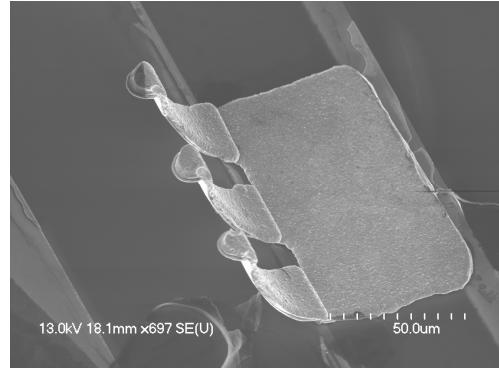


Fig. 5. SEM image of CMIs with 40  $\mu$ m in-line pitch

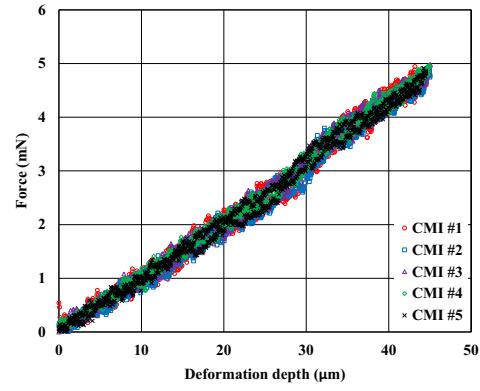


Fig. 6. Indentation graph of CMIs at five different locations

photoresist layer. To demonstrate this scalability, CMIs with an in-line pitch of 40  $\mu$ m were fabricated and are shown in Fig. 5. In addition, the upward-curved geometry of the CMIs, as shown by the side-profile of the CMIs in the SEM images, ensures that the contact pad remains in contact with the tip of the CMI during deflection.

### III. MEASUREMENTS

#### A. Mechanical Performance

In order to measure the mechanical compliance of CMIs, a Hysitron Triboindenter with a Cono-Spherical probe tip was used. The Cono-Spherical probe tip was positioned at the tip of the CMIs to ensure that the deformation force is applied at the tip of the CMIs. During each indentation cycle, the probe tip moves downward to a preset depth and then returns to its original position; during this motion, the reaction force versus indentation depth data of the CMIs is recorded. In this demonstration, five CMIs located in different areas of the same sample were indented downward by 45  $\mu$ m. Fig. 6 shows the measured compliance data. The CMIs can achieve 45  $\mu$ m of vertical elastic range of motion without plastic deformation. Moreover, the average measured compliance of the CMIs is 9.2 mm/N. In order to

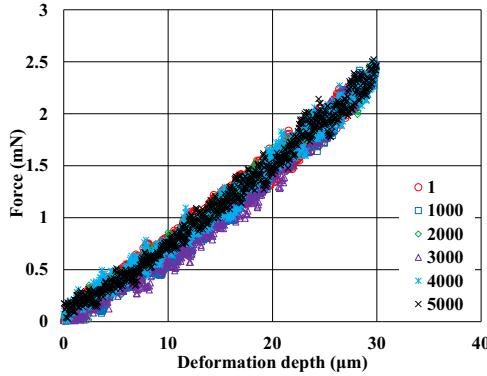


Fig. 7. 5,000 indentation cycles of a CMI

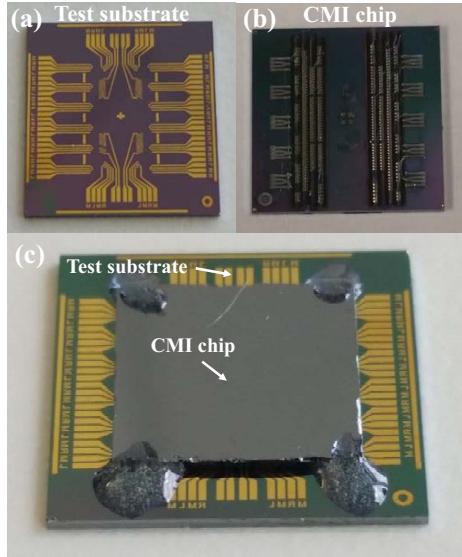


Fig. 8. Optical image of test substrate (a), CMI chip (b), and flip-chip bonded testbed (c)

gain some insight into the lifetime fatigue reliability of the CMIs, one of the CMIs on a new sample was consecutively indented for up to 5,000 indentation cycles and demonstrated the ability to recover its original height, as shown in Fig. 7. Since the compliance is inversely related to thickness, a wide range of compliance values can be achieved simply by adjusting the thickness of the CMIs; the thickness of CMIs can be easily adjusted by changing the electroplating time. Thus, a specific compliance can be attained depending on application requirements.

#### B. Electrical Performance

In order to measure the resistance of the CMIs after assembly, a chip containing CMIs was flip-chip bonded onto a silicon substrate with gold pads, as shown in Fig. 8. Finetech Fineplacer Lambda flip-chip bonder was used to

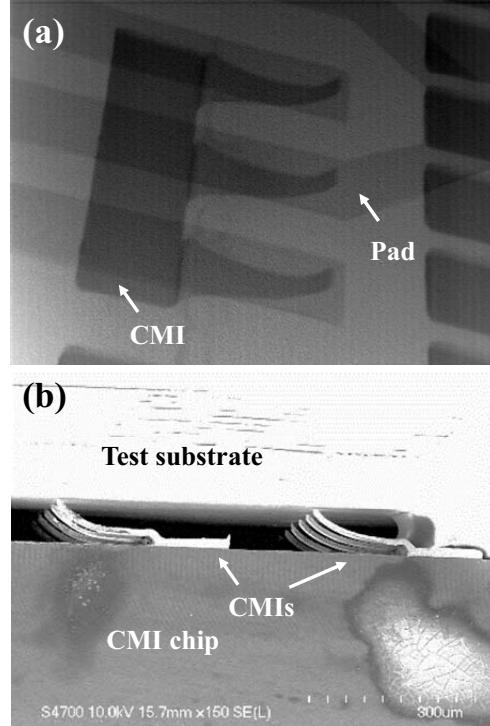


Fig. 9. X-ray image (a) and SEM image of cross section (b) of the flip-chip bonded testbed

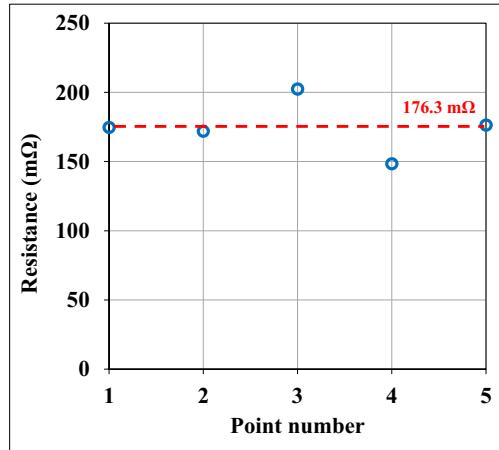


Fig. 10. Four-point resistance data of CMIs

assemble the chip and substrate; after aligning and bringing the chip into contact with the substrate, epoxy was applied to each of the four corners to secure the assembly (to facilitate measurements).

Dage X-Ray XD7600NT was used to verify the contact between the CMIs and the pads. As shown in Fig. 9 (a), the tips of the CMIs during four-point resistance measurements are positioned directly under the gold pads. An SEM image (Fig. 9 (b)) showing the cross-section of the assembled

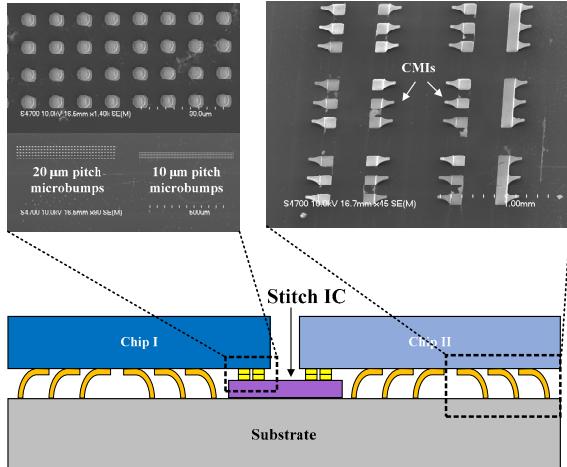


Fig. 11. Schematic of HIST platform and SEM images of microbumps and CMIs

sample shows that the CMIs are in contact with the test substrate.

Four-point probing was used to measure the resistance of the CMIs with a Karl-Suss probe station. Fig. 10 shows the measured resistance of the CMIs including the contact resistance. The average four-point resistance is 176.3 mΩ.

#### IV. HETEROGENEOUS INTEGRATION ENABLED BY CMIs

CMIs have been used in [22] as a key enabler for heterogeneous interconnect stitching technology (HIST). In this multi-die integration approach, a silicon die with fine-pitch traces (and circuits when needed) is placed between the adjacent chips that need to be interconnected. Fine-pitch microbumps (20 μm pitch) are utilized to interconnect adjacent dice via the silicon ‘stitch IC’ to provide high bandwidth signaling [22][22]. In addition to this, CMIs are used as interconnects between the chips and the substrate. Fig. 11 shows SEM images of the microbumps and CMIs used in the HIST platform. This methodology of integration circumvents the need for TSVs or making a cavity in the substrate for embedding the stitch IC; this is uniquely possible owing to the dense and large stand-off height of the CMIs to allow for the compensation of the height difference introduced by the stitch IC without embedding it in the substrate. Furthermore, the high elastic range of motion of the CMIs allows for compensating any CTE mismatch induced warpage thereby increasing mechanical reliability of the system. Fig. 12 shows an X-ray image of the assembled HIST testbed. The average post-assembly resistance of the microbumps was 117.32 μΩ, and the average resistance of the CMIs (including contact resistance) was 195.99 mΩ [22].

#### V. CONCLUSION

In this paper, dense, highly flexible CMIs are presented as a viable technology enabling future probe cards, sockets and heterogeneous integration. Owing to the scaling and advances in 2.5D and 3D integration, there are new

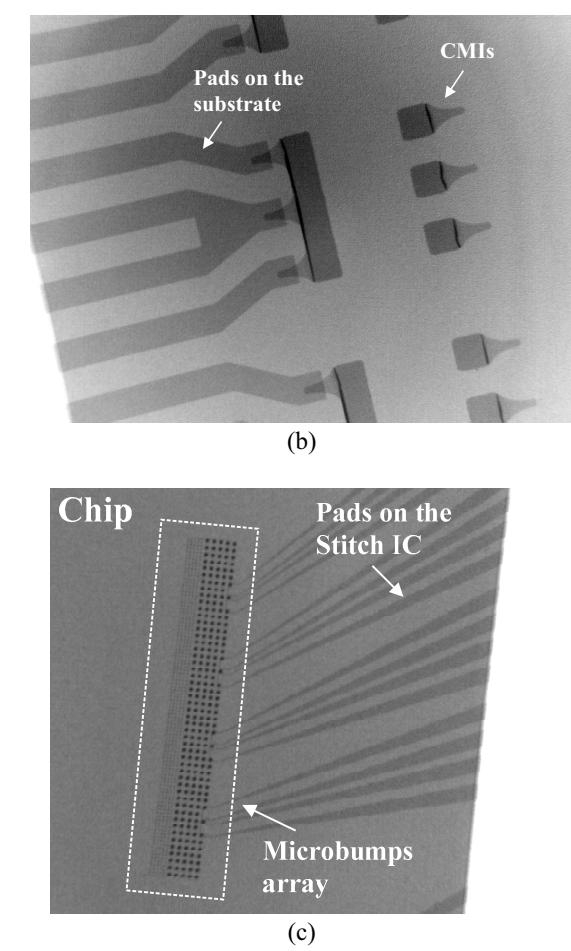
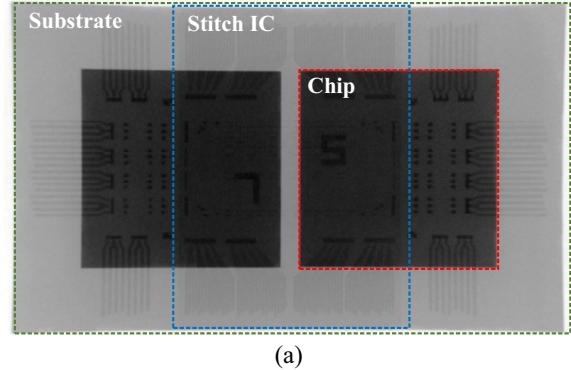


Fig. 12. X-ray image of the assembled HIST testbed (a), CMIs connected to the substrate (b), and microbumps bonded to the stitch IC (c)

challenges posed in each of these domains that trace their core need to the requirement of a highly compliant interconnect with high-density and low-contact resistance. The demonstrated CMIs address these challenges by providing 75 μm stand-off height and a vertical elastic range

of motion of up to 45  $\mu\text{m}$ . Furthermore, the in-line pitch of CMIs is shown to scale down to 40  $\mu\text{m}$ . Moreover, since CMIs are lithographically-defined, the pitch of the CMIs can be further scaled, and the maximum height of the CMIs can be adjusted accordingly by changing the thickness of the sacrificial photoresist layer. The compliance of the fabricated CMIs was measured to be 9.2 mm/N and they show elastic behavior even after 5,000 cycles of consecutive indentations. The average post-assembly resistance value of the CMIs, including the contact resistance, was 176.3  $\text{m}\Omega$ . These characteristics make CMIs particularly lucrative for the applications discussed in this paper and other emerging ones.

## REFERENCES

- [1] W. R. Mann, F. L. Taber, P. W. Seitzer, and J. J. Broz, "The leading edge of production wafer probe test technology," in *Proc. Int. Test Conf.*, Cincinnati, OH, 2004, pp. 1168-1195.
- [2] J. Novitsky and D. Pedersen, "FormFactor introduces an integrated process for wafer-level packaging, burn-in test, and module level assembly," in *Proc. Int. Symp. on Adv. Packag. Mat.*, Braselton, GA, 1999, pp. 226-231.
- [3] N. L. Tracy, R. Rothenberger, C. Copper, N. Cormand, G. Biddle, A. Matthews, and S. McCarthy, "Array sockets and connectors using MicroSpring<sup>TM</sup> technology," in *26<sup>th</sup> IEEE/CPMT Int. Electron. Manuf. Technol. Symp.*, Santa Clara, CA, 2000, pp. 129-140.
- [4] V. Pandey, S. Subramanian, S. Rangaraj, and T. Byquist, "Mechanical design and analysis of land grid array (LGA) sockets," in *ASME Int. Electron. Packag. Technic. Conf. and Exhib.*, San Francisco, CA, 2005, pp. 1005-1011.
- [5] V. Challa, L. D. Lopez, M. Osterman, and M. G. Pecht, "Stress relaxation testing of stamped metal land-grid-array sockets," *IEEE Trans. Dev. Mat. Rel.*, vol. 10, no. 1, pp. 55-61, Mar. 2010.
- [6] M. Zia, T. Chi, C. Zhang, P. Thadesar, T. Hookway, J. Gonzalez, T. McDevitt, H. Wang, and M. S. Bakir, "A microfabricated electronic microplate platform for low-cost repeatable bio-sensing applications," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, 2015, pp. 29.4.1-29.4.4.
- [7] S. C. Yang, C. J. Wu, Y. L. Hsiao, C. H. Tung, and D. C. H. Yu, "A flexible interconnect technology demonstrated on a wafer-level chip scale package," in *Proc. 65<sup>th</sup> IEEE Electron. Compon. and Technol. Conf.*, San Diego, CA, 2015, pp. 859-864.
- [8] I. Shubin, E. M. Chow, J. Cunningham, D. De Bruyker, C. Chua, B. Cheng, J. C. Knights, K. Sahasrabudhe, Y. Luo, A. Chow, J. Simons, A. V. Krishnamoorthy, R. Hopkins, R. Drost, R. Ho, D. Douglas, and J. Mitchell, "Novel packaging with rematable spring interconnect chips for MCM," in *Proc. 59<sup>th</sup> IEEE Electron. Compon. and Technol. Conf.*, San Diego, CA, 2009, pp. 1053-1058.
- [9] E. M. Chow, D. K. Fork, C. L. Chua, K. V. Schuylenbergh, and T. Hantschel, "Wafer-level packaging with soldered stress-engineered micro-springs," in *IEEE Trans. Advan. Packag.*, vol. 32, no. 2, pp. 372-378, May 2009.
- [10] N. Jackson and J. Muthuswamy, "Flexible Chip-Scale Package and Interconnect for Implantable MEMS Movable Microelectrodes for the Brain," in *Journal of Microelectromechanical Systems*, vol. 18, no. 2, pp. 396-404, April 2009.
- [11] J. Chang, M. Hung, B. Liao, N. Lin, A. Gattuso, and B. McHugh, "The challenges of LGA server socket trends," in *Proc. Pan Pacific Microelectron. Symp.*, Minneapolis, MN, 2013.
- [12] *Probing 25 $\mu\text{m}$ -diameter micro-bumps for Wide-I/O 3D SICs*, Haley Publishing Inc, Morgan Hill, CA, 2014.
- [13] M. Bakir, B. Dang, R. Emery, G. Vandentop, P. Kohl, and J. Meindl, "Sea of leads compliant I/O interconnect process integration for the ultimate enabling of chips with low-k interlayer dielectrics," *IEEE Trans. Adv. Packag.*, vol. 28, no. 3, pp. 488-494, Aug. 2005.
- [14] K. Kacker, G. C. Lo, and S. K. Sitaraman, "Low-K dielectric compatible wafer-level compliant chip-to-substrate interconnects," *IEEE Trans. Adv. Packag.*, vol. 31, no. 1, pp. 22-32, Feb. 2008.
- [15] Q. Zhu, M. Lunyu, and S. K. Sitaraman, " $\beta$ -Helix: A lithographybased compliant off-chip interconnect," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 3, pp. 582-590, Sep. 2003.
- [16] C. Zhang, H. S. Yang, and M. S. Bakir, "Mechanically flexible interconnects with highly scalable pitch and large stand-off height for silicon interposer tile and bridge interconnection," in *Proc. 64<sup>th</sup> IEEE Electron. Compon. and Technol. Conf.*, Orlando, FL, 2014, pp. 13-19.
- [17] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-Springs - innovative compliant interconnects for next-generation packaging," in *Proc. 52<sup>nd</sup> IEEE Electron. Compon. and Technol. Conf.*, San Diego, CA, 2002, pp. 1359-1365.
- [18] S. Koopman and J. Ferry, "Compliant connector for land grid array," U.S. Patent 6585527, Jul. 1, 2003.
- [19] B. DeFord, "Electronic assembly having a socket with features that ensure alignment in X- and Y-directions of a component held thereby," U.S. Patent 6848936, Feb. 1, 2005.
- [20] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632-1639, Oct. 2013.
- [21] E. Slavcheva, W. Mokwa, and U. Schnakenberg, "Electrodeposition and properties of NiW films for MEMS application," *Electrochim. Acta*, vol. 50, no. 28, pp. 5573-5580, Sep. 2005.
- [22] X. Zhang, P. K. Jo, M. Zia, and M. S. Bakir, "Heterogeneous interconnect stitching technology with compressible microInterconnects for dense multi-die integration," in *IEEE Electron Devices Letters*, vol. 38, no. 2, pp. 255-257, Feb. 2017.